**Lab 3: Combinational Design**

**Primary Objectives**

1. Analyze and design a combinational system

2. Implement the system using the Logisim software

3. Test to verify the functionality of said system

*Objective 1 Design*

There are four inputs and two outputs in this project: A0, A1, B0, and B1 for the inputs, and C0 and C1 for the outputs. The system is supposed to work as a 2-bit maximum value selector. This means that the output pair should match whichever pair of inputs (A1A0/B1B0) has the larger binary value representation.

If this system is functional, the truth table should look like this:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A1 | A0 | B1 | B0 | C1 | C0 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | **1** |
| 0 | 0 | 1 | 0 | **1** | 0 |
| 0 | 0 | 1 | 1 | **1** | **1** |
| 0 | 1 | 0 | 0 | 0 | **1** |
| 0 | 1 | 0 | 1 | 0 | **1** |
| 0 | 1 | 1 | 0 | **1** | 0 |
| 0 | 1 | 1 | 1 | **1** | **1** |
| 1 | 0 | 0 | 0 | **1** | 0 |
| 1 | 0 | 0 | 1 | **1** | 0 |
| 1 | 0 | 1 | 0 | **1** | 0 |
| 1 | 0 | 1 | 1 | **1** | **1** |
| 1 | 1 | 0 | 0 | **1** | **1** |
| 1 | 1 | 0 | 1 | **1** | **1** |
| 1 | 1 | 1 | 0 | **1** | **1** |
| 1 | 1 | 1 | 1 | **1** | **1** |

Table 1 Design

*Objective 2 Implementation*

Figure 1 shows one way the system could be implemented via Logisim. Both outputs in this system are labeled with the Boolean expression they are represented by. Therefore, the Boolean expressions that represent this circuit are C1 = A1 + B1 and C0 = ~A1 B0 + B1 B0 + A0 ~B1 + A1 A0.

A diagram of a circuit

Description automatically generated

Figure 1 Implementation

*Objective 3 Testing*

To test this circuit, I tried each individual combination of inputs manually in the circuit. I then checked their outputs to see if they represented the maximum value of the inputs and, consequently, matched up with the truth table. The testing was completely successful, ensuring that the circuit works as intended.

**Conclusion**

The lab went smoothly with no issues. The initial table made from the problem description matches the table generated after the circuit was designed and implemented in Logisim. Testing also showed that the circuit works as intended. Therefore, the circuit was designed properly, and the lab was successful.